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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/755,254 | 01/04/2001 | William Joshua Price | M-8504 US | 5201 |

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| EXAMINER | |
|---|---|
| CHANG, ERIC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2116 | |

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/755,254 | PRICE, WILLIAM JOSHUA | |
| | Examiner | Art Unit | |
| | Eric Chang | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-26 are pending.

### *Claim Rejections - 35 USC § 103*

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent U.S. Patent 6,260,079 to White, in view of U.S. Patent 4,220,876 to Ray.

4. As to claim 1, White discloses a device comprising a controller powered by a voltage circuit and coupled to an internal bus [FIG. 10, and col. 15, lines 38-56]. White teaches that a plurality of such devices may further be coupled to an external SCSI bus [FIG. 5, elements 513-515 and 518]. Therefore, White teaches a first device comprising a first controller powered by a first voltage circuit and coupled to a first bus, and a second device comprising a second controller powered by a second voltage circuit and coupled to a second bus, substantially as claimed, and that the two devices are further coupled to an external bus.

White teaches all of the limitations of the claim but does not teach that a first switch is coupled between the buses to decouple the first and second buses when a voltage falls below a predetermined threshold.

Ray teaches a switch operative to decouple a device from a bus when a voltage falls below a predetermined threshold [Abstract]. When an un-powered device taught by

White is decoupled from the external bus using the teachings of Ray, the internal bus of the un-powered device is thereby decoupled from the internal buses of other devices on the external bus, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the bus decoupling means as taught by Ray. Ray teaches that one of ordinary skill in the art would have been motivated to do so that the loss of power, either intentional or accidental, to a device on the bus would not affect the electrical load on the bus [col. 1, lines 35-57].

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of providing resilient and fault-tolerant performance for devices on a bus. Moreover, the bus decoupling means taught by Ray would improve the robustness of White because it electrically isolates un-powered devices, thereby preventing bus performance degradation and a concomitantly negative impact on the operation of other devices on the bus.

5. As to claims 2-4, 6-8, 10-13, 15-18, 20-22 and 24-26, White discloses a bus coupled to a first plurality of elements, including at least one of a temperature sensor, a memory, a backplane controller, a port bypass circuit, an I/O expansion slots for disk drives, and at least one power supply [col. 20, lines 64-67, and col. 21, lines 1-26]. It would further be well known to one of ordinary skill in the art that a battery can be used as a power supply, substantially as claimed.

6. As to claims 5, 9, 14, 19 and 23, White discloses devices comprising a controller powered by a first voltage circuit and coupled to an internal bus. Ray discloses a switch operable to decouple devices from an external bus, and the internal buses of said devices from each other when the voltage output from a power circuit falls below a predetermined threshold. Because White and Ray teach that the buses coupled to a controller may be decoupled when the voltage output from a power circuit falls below a predetermined threshold, it would be obvious to one of ordinary skill in the art that White and Ray further teach that any number of buses coupled to a controller may likewise be decoupled by such switch means. Therefore, White and Ray teach a second, third and fourth switch for decoupling a third, fourth, fifth, sixth and seventh bus coupled to controllers, substantially as claimed.

***Response to Arguments***

7. Applicant's arguments filed on January 19, 2005 have been fully considered but they are not persuasive.

8. In the remarks, applicants argued in substance that Ray does not teach or suggest that circuit 44 does not decouple instrument 10 from either bus 50 either physically or electrically. But Ray teaches a circuit that renders devices connected thereto non-conductive and thereby electrically isolates them from the bus [Abstract]. Specifically, Ray teaches that circuit 44 is interposed between a bus input terminal 46 and an external bus 50 [col. 3, lines 5-11].

9. Furthermore, Ray teaches the operation of the circuit [col. 4, lines 1-40], and as Applicant agrees, operation of the circuit when the voltage output from a voltage circuit falls below a predetermined threshold [col. 4, lines 13-40]. With particular regard to the decoupling of the bus, Ray teaches that when the voltage output falls below said threshold, node 48 presents a high impedance to the bus 50 [col. 4, lines 34-40], preventing circuit 44 from loading the bus. Because node 48 is presents a high impedance, no electrical current may pass from bus input terminal 46, or circuits connected thereto, to bus 50, thereby electrically decoupling and isolating any such circuits from bus 50, substantially as claimed.

10. Ray discloses the process by which node 48 presents a high impedance [col. 4, lines 13-40], wherein the voltage threshold is detected by diodes 68, 70 and 72, which in turn control transistor switch 64. In summary, when the voltage falls below the threshold, current is prevented from flowing through segment 52-62, comprising node 48, thereby electrically decoupling and isolating circuits coupled to node 48 from bus 50. This not only electrically decouples resistors 58 and 60, as admitted by Applicant, but also any other circuits coupled to node 48, such as those coupled to bus input terminal 46. The effect of high impedance and concomitant electrical isolation of node occurs due to the nature of current flow in the circuit when transistor switch 64 is rendered non-conductive, as is well known to one of ordinary skill in the art.

11. In the remarks, applicants argued in substance that Ray does not teach or suggest that a switch that physically or electrically isolates two buses. But Ray teaches that

electrical systems connected to the bus input terminal 46 are electrically isolated from bus 50, such that elements coupled to node 48 do not load bus 50 when transistor switch 64 is deactivated following a predetermined voltage drop [col. 4, lines 34-40]. Ray further teaches that such electrical systems comprise any number of other systems or subsystems [col. 5, lines 4-27], such as another bus, substantially as claimed.

### *Conclusion*

12. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

February 14, 2005
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